Photoelectric Conversion Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a photoelectric conversion apparatus having photoelectric conversion elements arrayed in a matrix and being capable of obtaining a high-quality image.

Related Background Art

Fig. 1 is a diagram for explaining a conventional photoelectric conversion apparatus. Referring to Fig. 1, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4 × 4 elements in Fig. 1). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2,

the vertical selection switch MOS 3, and load power supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective photoelectric conversion elements sequentially turn on the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in

units of pixels.

In the prior art described above, since finite resistances are distributed in the vertical output lines 6, shading in the vertical direction occurs in the signals due to potential drops across the resistances. For descriptive convenience, one pixel and its peripheral portion are illustrated in Fig. 2. Referring to Fig. 2, a resistance 201 is distributed on the vertical output line 6. Let M rows of pixels be present, and r1 be the resistance value of the vertical output line per row. Then, the total resistance between the pixels on the Kth row and the horizontal transfer MOS switch 10 is defined as:

$$r1 \times K \quad (1 \leq K \leq M) \qquad \ldots(1)$$

Let Ia, Rm, Vth0, and Vsig0 be the current flowing through the load power supply 7, the series resistance of the vertical selection switch MOSs 3, the threshold voltage of the source follower input MOS 2, and the signal voltage on the gate of the source follower input MOS 2, respectively. Then, a signal Vsig1 current-amplified and read by the source follower circuit is defined as:

$$Vsig1 = Vsig0 - Vth0 - Ia \times Rm - Ia \times r1 \times K \quad (1 \leq K \leq M) \qquad \ldots(2)$$

That is, even if the identical signal voltages Vsig0 is induced at the pixels, the voltages Vsig1 read in units of rows have differences due to voltage drops by the

resistances r1 of the vertical output lines 6, thus causing vertical shading. The image quality is greatly deteriorated.

In recent years, the number of pixels increases and the size decreases in the development of photoelectric conversion apparatuss. The wirings used in the photoelectric conversion apparatuss tend to be thin and long. Voltage drop by the resistance r1 of the vertical output line 6 poses a serious problem.

Another problem is posed by different dynamic ranges of the source follower circuit in units of rows because a finite resistance is distributed on the power supply line 4. This problem will be described with reference to Fig. 2. A resistance 202 in Fig. 8 is distributed on the power supply line 4. Let M rows of pixels be present, and r2 be the resistance value of the power supply line per row. Then, the total resistance between the pixels on the Kth row and the power supply terminal 5 is:

$$r2 \times K \quad (1 \leq K \leq M) \qquad \ldots(3)$$

Letting Vd be the voltage of the power supply terminal 5, the source follower input MOS 2 must operate as a pentode in order to operate the source follower circuit as a linear amplifier. A condition for this is given by:

$$Vd - Ia \times r2 \times K > Vsig0 - Vth0 \quad (1 \leq K \leq M) \qquad \ldots(4)$$

The above condition can be rewritten as:

$$Vsig0 < Vd + Vth0 - Ia \times r2 \times K \ (1 \leq K \leq M) \quad ...(5)$$

The signal voltage values not satisfying the above condition are different depending on the rows. That is, the signals have different dynamic ranges.

This results in saturation voltage shading or output shading on the small-light-amount characteristic side due to a combination with the polarities of the photodiode 1, thereby greatly degrading the image quality.

SUMMARY OF THE INVENTION

It is an object of the present invention to prevent degradation of image quality in a photoelectric conversion apparatus.

In order to achieve the above object, according to the first embodiment, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, amplification means, including load means arranged in units of vertical output lines, for amplifying signal charges accumulated in the photoelectric conversion elements mounted in the plurality of rows, vertical scanning means for sequentially scanning signals amplified by the amplification means to read the signals onto the vertical output lines, and horizontal scanning means for sequentially scanning the signals amplified by the amplification means to read the

signals onto horizontal output lines, wherein the load means are located on a side vertically opposite to a direction of signal output from the amplification means.

According to another embodiment, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, amplification means, including load means arranged in units of vertical output lines, for amplifying signal charges accumulated in the photoelectric conversion elements mounted in the plurality of rows, vertical scanning means for sequentially scanning signals amplified by the amplification means to read the signals onto the vertical output lines, and horizontal scanning means for sequentially scanning the signals amplified by the amplification means to read the signals onto horizontal output lines, wherein the load means are located on vertically the same side as a direction of outputting the signals from the amplification means, and some of the signals from the amplification means are output in an opposite direction to the direction of signal output.

According to still another embodiment, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, amplification means for amplifying

signal charges accumulated in the photoelectric conversion elements mounted in the plurality of rows, vertical scanning means for sequentially scanning signals amplified by the amplification means to read the signals onto the vertical output lines, horizontal scanning means for sequentially scanning the signals amplified by the amplification means to read the signals onto horizontal output lines, and power supply means for supplying power supply voltages to the amplification means, wherein one of the power supply means is located on a side vertically opposite to a direction of signal output from the amplification means.

According to still another embodiment of the present invention, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, output means for outputting as voltage signals signal charges accumulated in the photoelectric conversion elements mounted on the plurality of rows, vertical scanning means for sequentially scanning the voltage signals from the output means to read the voltage signals onto vertical output lines, horizontal output means for sequentially scanning the voltage signals on the vertical output lines to read the voltage signals onto horizontal output lines, and shading correction means for correcting shading resulting from a voltage

signal level difference between the photoelectric conversion elements on different rows, which is output from the output means.

With the above arrangements, a high-quality photoelectric conversion apparatus can be provided.

The above and other objects, features, and advantages of the present invention will be apparent from the detailed description of the preferred embodiments taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram for explaining a conventional photoelectric conversion apparatus;

Fig. 2 is a circuit diagram for explaining the operation of the conventional photoelectric conversion apparatus;

Fig. 3 is a diagram for explaining the operation of the first embodiment of the present invention;

Fig. 4 is a circuit diagram for explaining the operation of the first embodiment of the present invention;

Fig. 5 is a diagram for explaining the second embodiment of the present invention;

Fig. 6 is a diagram for explaining the third embodiment of the present invention;

Fig. 7 is a diagram for explaining the fourth

embodiment of the present invention; and

Fig. 8 is a diagram for explaining the fifth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 is a diagram for explaining the first embodiment of the present invention. Constant current sources 7 are located on the side vertically opposite to the direction of outputting signal voltages from a source follower circuit. Referring to Fig. 3, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4 × 4 elements in Fig. 3). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2, the vertical selection switch MOS 3, and load power

supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective photoelectric conversion elements sequentially turn on the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in units of pixels. An amplifier such as a MOS amplifier

having a high input impedance is preferable as the output amplifier 12.

Fig. 4 shows one pixel and its peripheral portion for illustrative convenience. Referring to Fig. 4, a resistance 401 is present between the source follower and the constant current source 7. A steady current of the constant current source 7 flows into the constant current source 7 via this resistance 401. A resistance 201 is present between the source follower and the output terminal.

A voltage Vsig1' at the output terminal of the source follower is given by:

$$Vsig1' = Vsig0 - Vth0 - Ia \times Rm \quad \ldots(6)$$

This value is a constant value which is determined by the design values of the transistor and the steady current.

As previously described, the steady current Ia flows into the constant current source 7 via the resistance 401, and the voltages Vsig1 at the connection points between the constant current sources 7 and the resistances 401 have potential differences in units of pixel rows due to the presence of the resistances 401, as indicated by equation (2) above.

The load power supplies 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the source follower circuits. Hence, only a transient current in the initial read

period flows across the resistance 201, and no steady current flows across it. A voltage Vsig2 at the connection point between the resistance 201 and the horizontal transfer MOS switch 10 is given by:

$$Vsig2 = Vsig1' \quad \ldots(7)$$

No potential effect occurs by resistance. Therefore, vertical shading can be greatly reduced, and image quality can be improved.

In this embodiment, the source follower circuit using a constant current type load has been described above. The present invention, however, is not limited to this. The same effect as described can be obtained by using a resistance type circuit. This also holds true for the use of an inverting amplifier type circuit which is not a source follower circuit but a circuit for inverting and amplifying the charges accumulated in a photoelectric conversion element and outputting the charges onto a vertical output line, as disclosed in U.S.P. No. 5,698,844.

In addition, the same effect can be also obtained even when a signal is stored temporarily in a capacity and then read out therefrom, instead of being input into the amplifier directly.

In this embodiment, the shading correction means is an arrangement in which the constant current sources 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the

source follower circuits. This arrangement has a function of correcting shading arising from level differences of signals output from the source follower circuits of the respective rows.

In this embodiment, the current output means is an arrangement in which the constant current sources 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the source follower circuits.

The above arrangement has a function of flowing currents on the vertical output lines to the constant current source side but not in the direction in which signals are output from the source follower circuits.

Fig. 5 is a chart for explaining the second embodiment of the present invention. Constant current sources are located on vertically the same side as a direction of outputting signal voltages from source follower circuits, and at the same time, the signal voltages in units of rows are alternately output in opposite directions.

Referring to Fig. 5, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4 × 4 elements in Fig. 5). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is

connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induces at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective photoelectric conversion elements sequentially turn on

the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in units of pixels.

The horizontal transfer MOS switches 10 are connected to every other vertical output lines 6, and each horizontal scanning circuit 13 outputs a signal from the corresponding horizontal transfer MOS switch 10 to the corresponding horizontal output line 11 for each vertical output line 6. The constant current sources 7 serving as the loads of the source follower circuits are connected to the sources of the horizontal transfer MOS switches 10 on the vertical output line 6 side. The resistance values of the vertical output lines are different depending on the locations of the vertical gate lines 8. The horizontal scanning circuits 13 are arranged on the two terminals of each vertical output line 6. The horizontal scanning circuits 13 on the two terminals synchronously operate to turn on each horizontal transfer MOS switch 10 in units of vertical output lines 6. Each horizontal

scanning circuit 13 reads an optical charge signal from the photoelectric conversion element 1 to the corresponding horizontal output line 11, thereby outputting the signal from the corresponding output amplifier 12. In this case, the horizontal transfer MOS switches 10 at the two terminals are turned on to increase the read rate.

Although not shown, the output signals from the output amplifiers 12 at the two terminals may be concatenated as a time-serial image signal sequence and output as a video signal via a sample/hold circuit, a shading correction circuit, and the like.

With the above arrangement, assume a photoelectric conversion apparatus having elements at M rows and N columns. A signal voltage read from a pixel at the Kth row and Lth column ($1 \leq K \leq M$, $1 \leq L \leq N$) is given by:

$$VsigKL = Vsig0 - Vth0 - Ia \times Rm - Ia \times r1 \times K \quad (1 \leq K \leq M) \quad ...(8)$$

(where Rm is the series ON resistance value of the vertical selection switch MOSs 3, r1 is the resistance value of the vertical output line 6 per row, Vsig0 is the output voltage of the photoelectric conversion element 1, Vth0 is the threshold voltage of the source follower input MOS 2, and Ia is the current of the constant current source 7). A signal voltage read from a pixel at the Kth row and (L+1)th column ($1 \leq K \leq M$, $1 \leq L \leq N$) is influenced by a different resistance value

because the voltage extraction direction is reversed, and becomes:

$$VsigKL+1 = Vsig0 - Vth0 - Ia \times Rm - Rm - Ia \times r1 \times (M - K) \quad (1 \leq K \leq M) \quad ...(9)$$

As can be apparent from the above equation, for example, when odd-numbered columns are taken into consideration, shading has occurred in this embodiment as in the conventional case, but shading opposite to that of the odd-numbered columns has occurred in even-numbered columns, thereby averaging and canceling shading and hence greatly improving the image quality.

In practice, a relevant external circuit can be mounted outside or inside the device to add or average adjacent signals to further reduce shading. In a photoelectric conversion apparatus for sensing a color image using color filters of, e.g., complementary colors, processing for adding and reading adjacent signals is generally performed by adding and reading signals of adjacent pixels, and reconstructing a video signal by external matrix operations. In this case, the use of the arrangement of the present invention allows reduction in shading without causing any trouble.

This embodiment has exemplified a case in which constant current sources are alternately connected to the columns. The constant current sources may be connected to every two or three columns, depending on

the degree of shading, to obtain the same effect as described above. Alternatively, constant current sources may be alternately connected to the columns at only the central portion of the light-receiving section of a photoelectric conversion apparatus.

In this embodiment, a source follower circuit using a constant current load has been described. However, the present invention is not limited to this. The same effect as in this embodiment can be obtained with the use of a resistance type load. This also holds true for the use of an inverting amplifier type circuit which is not a source follower circuit but a circuit for inverting and amplifying the charges accumulated in a photoelectric conversion element and outputting the charges onto a vertical output line, as disclosed in U.S.P. No. 5,698,844.

In addition, the same effect can be also obtained even when a signal is stored temporarily in a capacity and then read out therefrom, instead of being input into the amplifier directly.

In this embodiment, the shading correction means is an arrangement in which the constant current sources 7 are located on vertically the same side as the direction of outputting the signal voltages from the source follower circuits, and at the same time, the signal voltages in units of rows are alternately output in opposite directions. This arrangement has a

function of correcting shading resulting form level differences of signals output from the source follower circuits of the respective rows.

In this embodiment, the current output means is an arrangement in which the constant current sources 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the source follower circuits, and at the same time, the signal voltages in units of rows are alternately output in opposite directions. In this arrangement, the level differences of voltage signals, between different rows, that are output from the source follower circuits are alternately opposite to each other.

Fig. 6 is a diagram for explaining the third embodiment of the present invention. The power supply terminals of source follower circuits are alternately arranged at vertically opposite positions.

Referring to Fig. 6, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4 × 4 elements in Fig. 6). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power

supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit. The power supplies of the respective source follower circuits are connected to the power supply lines 4 in units of rows. The power supply lines 4 are alternately connected to the power supply terminals 5.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective

photoelectric conversion elements sequentially turn on the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in units of pixels.

With the above arrangement, the dynamic range of a signal read from a pixel at the Kth row and Lth column ($1 \leq K \leq M$, $1 \leq L \leq N$) falls within the range:

$$VsigKL < Vd + Vth0 - Ia \times r2 \times K \quad (1 \leq K \leq M) \quad \ldots(10)$$

(where Vd is the power supply voltage, Vth0 is the threshold voltage of the source follower input MOS 2, and r2 is the resistance value between the drain of the source follower input MOS 2 corresponding to each vertical gate line 8 of the power supply line 4 and the drain of the source follower input MOS 2 corresponding to the next vertical gate line 8). At this time, the dynamic range of a signal read from a pixel at the Kth row and (L+1)th row ($1 \leq K \leq M$, $1 \leq L \leq N$) is:

$$VsigKL < Vd + Vth0 - Ia \times r2 \times (M - K) \quad (1 \leq K \leq M) \quad \ldots(11)$$

As is apparent from the above condition, for example, when odd-numbered columns are taken into consideration, shading of the saturation voltage of the photoelectric conversion characteristics of the photoelectric conversion element 1 or small-light-amount side output shading has occurred in this embodiment as in the conventional case, but shading opposite to that of the odd-numbered columns has occurred in even-numbered columns, thereby averaging and canceling shading and hence greatly improving the image quality.

This embodiment has exemplified a case in which constant current sources are alternately connected to the columns. The constant current sources may be connected to every two or three columns, depending on the degree of shading, to obtain the same effect as described above. Alternatively, constant current sources may be alternately connected to the columns at only the central portion of the light-receiving section of a photoelectric conversion apparatus.

In this embodiment, a source follower circuit using a constant current load has been described. However, the present invention is not limited to this. The same effect as in this embodiment can be obtained with the use of a resistance type load. This also holds true for the use of an inverting amplifier type circuit which is not a source follower circuit but a circuit for inverting and amplifying the charges

accumulated in a photoelectric conversion element and outputting the charges onto a vertical output line, as disclosed in U.S.P. No. 5,698,844.

In addition, the same effect can be also obtained even when a signal is stored temporarily in a capacity and then read out therefrom, instead of being input into the amplifier directly.

In this embodiment, the shading correction means is an arrangement in which the power supply terminals 5 of the source follower circuits are alternately located in the vertically opposite directions of columns. This arrangement has a function of correcting shading resulting from level differences of signals output from the source follower circuits of the respective rows.

In this embodiment, the power supply voltage supply means is an arrangement in which the power supply terminals 5 of the source follower circuits are alternately located in the vertically opposite directions of columns. This arrangement has a function of alternately reversing the directions of vertically reducing the power supply voltage supply amounts in units of columns in order to output signal voltages from the source follower circuits.

When a current read type amplifier is used, a new effect, i.e., reduction in output current shading can be obtained.

Fig. 7 is a diagram for explaining the fourth

embodiment of the present invention. Referring to Fig. 7, a reset switch 701 removes the charge accumulated in a photoelectric conversion element 1. The source of the reset switch 701 is connected to the photoelectric conversion element 1, and the drain of the reset switch 701 is connected to a power supply line 4 common to the source follower circuit. A reset gate line 702 controls the reset switch 701. The pixel arrangement of this embodiment is applicable to the first to third embodiments. With this pixel arrangement, as compared with the first to third embodiments, the reset voltage of the photoelectric conversion element 1 can be accurately controlled. DC level variations of the signal voltages produced by reset voltage variations, and any after image produced by the reset voltage remaining upon irradiation of strong light can be reduced. In particular, when this arrangement is applied to the third embodiment described above, power supply terminals 5 are alternately located in the vertically opposite directions in units of columns or in units of a plurality of columns, thereby greatly reducing signal voltage shading.

Fig. 8 is a diagram for explaining the fifth embodiment of the present invention. Referring to Fig. 8, a charge transfer switch 801 perfectly depletes and transfers the signal charge from a photoelectric

conversion element 1 to a source follower input MOS 2. A transfer gate line 802 controls the transfer switch 801. In general, to increase the sensitivity of the photoelectric conversion apparatus, the size of the photoelectric conversion element 1 is increased and the conversion amount is increased in converting an optical signal into an electrical signal. The parasitic capacitance value of the gate of the source follower input MOS 2 increases accordingly, the read rate lowers, and the sensitivity cannot efficiently increase. With the arrangement of this embodiment, however, the capacitance value of the input gate of the source follower input MOS 2 is designed to be smaller than that of the photoelectric conversion element 1 (e.g., a photodiode), and perfect depletion transfer is performed to increase the sensitivity.

As shown in Fig. 8, a vertical selection switch MOS 3 is inserted between a power supply line 4 and the source follower input MOS 2, and the voltage drop accounted for by the resistance of the vertical selection switch MOS 3:

$$Ia \times Rm \qquad \ldots(12)$$

in equation (2) can be eliminated, thereby obtaining a wide dynamic range.

The pixel arrangement of this embodiment can be applied to the first to third embodiments to obtain the same effect as described above.

In the first to fifth embodiments, the same effect can be obtained regardless of the NMOS or PMOS transistor. The above embodiments can be combined to further reduce or prevent occurrence of shading. For example, when the case in which different power supply terminals located at two terminals of the power supply lines shown in the third embodiment is combined with the case in which the horizontal output lines 11 are located at two terminals of the horizontal output lines 11 as shown in the second embodiment, both shading attributed to the resistance of the vertical output line and shading attributed to the resistance of the power supply line can be eliminated.

The present invention is not limited to the pixel structures shown in the first to fifth embodiments. For example, an arrangement in which the charge accumulated in the photoelectric conversion element is not amplified before being output, i.e., the charge is output without amplification can be employed. The transistor is not limited to the MOS element, but can be an SIT or BASIS element.

As has been described above, according to the first to fifth embodiments, vertical shading of the output signals from the photoelectric conversion apparatus can be reduced.

In addition, vertical saturation voltage shading of the output signal from the photoelectric conversion

apparatus can also be reduced, and the dynamic range of the output from each photoelectric conversion element can be widened.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.